WHAT IS CLAIMED IS:

1. A method for testing a sense amplifier in a dynamic memory circuit having at the sense amplifier connected to a first bit line pair via a first switching device and to a second bit line pair via a second switching device and first memory cells arranged at crossover points between first word lines and one of the bit lines of the first bit line pair and second memory cells being arranged at crossover points between second word lines and one of the bit lines of the second bit line pair, comprising:

writing data to the first and the second memory cells to be subsequently read out;

during read-out of one of the first memory cells, activating a relevant first word line and the first switching device while the second switching device is closed; and

during read-out of one of the second memory cells, activating a relevant second word line and the second switching device while the first switching device is closed;

wherein one of the first and one of the second memory cells are read in a sequence such that the first and the second switching devices are switched multiply during testing of the first and second memory cells.

2. The method of claim 1, wherein the first and the second memory cells are read alternately.

3. The method of claim 2, wherein the first and second memory cells are addressed by a plurality of addresses and the first and second switching devices are driven by a least significant address bit of respective addresses.

4. The method of claim 1, wherein charge potentials of the bit lines of the first bit line pair are equalized before activation of one of the first word lines, and wherein charge potentials of the bit lines of the second bit line pair are equalized before activation of one of the second word lines.

5. A testing system, comprising:

a test circuit for testing a sense amplifier of a memory circuit;

a first switching device connected to a first bit line pair and the sense amplifier and a second switching device connected to a second bit line pair and the sense amplifier; and

first memory cells arranged at crossover points between first word lines and one of the bit lines of the first bit line pair and second memory cells being arranged at crossover points between second word lines and one of the bit lines of the second bit line pair;

wherein the test circuit is configured to write test data to the first and the second memory cells and subsequently to read out said test data;

the test circuit , during the read-out of one of the first memory cells, activating the relevant first word line, activating the first switching device and closing the second switching device;

the test circuit, during the read-out of one of the second memory cells, activating the relevant second word line, closing the first switching device and activating the second switching device; and

wherein the test circuit controls the read-out of the first and the second memory cells such that the first and the second switching device are switched multiply during testing of the first and second memory cells.

6. The testing system of claim 5, wherein the test circuit controls the read-out such that the first and the second memory cells are read alternately.

7. The test system of claim 5, further comprising:

a first equalization device connected to the first switching device and the first bit line pair; and

a second equalization device connected to the second switching device and the second bit line pair.

8. The test system of claim 7, wherein the first equalization and second equalization devices are configured to equalize charges on the first and second bit line pairs respectively, before and after read-out of the first and second memory cells respectively.

9. The test circuit of claim 8, further comprising a control device connected to the first and second switching devices and the first and second equalization devices.

10. The test system of claim 9, wherein the control device provides signals to selectively activate and deactivate the first and second switching devices and the first and second equalization devices.

11. A method for testing a memory circuit, comprising:

writing data to first memory cells and second memory cells, the first memory cells arranged at crossover points between first word lines and one of first bit lines, the second memory cells arranged at crossover points between second word lines and one of second bit lines;

reading data from one of the first memory cells by activating a first word line and a first switching device connected to a sense amplifier and the first bit lines;

reading data from one of the second memory cells by activating a second word line and a second switching device connected to the sense amplifier and the second bit lines; and

repeating the reading steps for remaining first and second memory cells.

12. The method of claim 11, wherein the second switching device is deactivated while data is being read from the first memory cells and the first switching device is deactivated while data is being read from the second memory cells.

13. The method of claim 11, further comprising:

prior to reading data from each of the first memory cells, activating a first equalization device connected to the first bit lines to equalize charge potentials of the first bit lines; and

prior to reading data from each of the second memory cells, activating a second equalization device connected to the second bit lines to equalize charge potentials of the second bit lines.

14. The method of claim 13, wherein a control device sends signals to selectively activate and deactivate the first and second switching devices.

15. The method of claim 14, wherein the control device sends signals to selectively activate and deactivate the first and second equalization devices.

16. The method of claim 15, wherein a test circuit controls the testing of the memory circuit and the operation of the control device.

17. The method of claim 11, wherein the first and second memory cells are addressed by a plurality of addresses and the first and second switching devices are driven by a least significant address bit of the addresses.

18. The method of claim 16, wherein the first bit lines and the second bit lines are redundant bit lines.

19. The methods of claim 11, wherein each of the first memory cells are read sequentially.

20. The methods of claim 11, wherein individual first memory cells are read alternately with individual second memory cells.